PASS: Exploiting Post-Activation Sparsity in Streaming Architectures for CNN Acceleration

Alexander Montgomerie-Corcoran*, Zhewen Yu*, Jianyi Cheng and Christos-Savvas Bouganis Imperial College London, UK

{alexander.montgomerie-corcoran15, zhewen.yu18, jianyi.cheng17, christos-savyas.bouganis}@imperial.ac.uk

Abstract—With the ever-growing popularity of Artificial Intelligence, there is an increasing demand for more performant and efficient underlying hardware. Convolutional Neural Networks (CNN) are a workload of particular importance, which achieve high accuracy in computer vision applications. Inside CNNs, a significant number of the post-activation values are zero, resulting in many redundant computations. Recent works have explored this post-activation sparsity on instruction-based CNN accelerators but not on streaming CNN accelerators, despite the fact that streaming architectures are considered the leading design methodology in terms of performance. In this paper, we highlight the challenges associated with exploiting post-activation sparsity for performance gains in streaming CNN accelerators, and demonstrate our approach to address them. Using a set in of modern CNN benchmarks, our streaming sparse accelerators achieve 1.41 \times to 1.93 \times efficiency (GOP/s/DSP) compared to state-

of model if ChA betchmarks, our streaming sparse accelerators achieve 1.41× to 1.93× efficiency (GOP/s/DSP) compared to state-of-the-art instruction-based sparse accelerators.
I. INTRODUCTION
Despite the successes of Transformers [1], CNNs [2], [3] are still the de-facto method for many vision tasks. The Rectified Linear Unit (ReLU) activation operation is ubiquitous within CNNs as it introduces non-linearities, increasing the network capacity. ReLU operation clamps all negative values in the feature maps to zero, leading to many redundant operations, a property referred to as post-activation sparsity. As an alternative to post-activation sparsity, weight sparsity can be induced through the pruning of near-zero parameters [4]. However, weight sparsity exploitation incurs an accuracy penalty, and requires re-training to recover accuracy losses. On the contrary, post-activation sparsity exploitation does not introduce approximations in the computations, and offers a large potential for performance gains.
Recent works have explored post-activation sparsity on instruction-based CNN accelerators [5], [6], where the computation of layers is time-multiplexed in hardware. As feature maps are repeatedly read to and from off-chip memory during execution, they are encoded to reduce memory foot-activation encoded to reduce memory foot-activatio

during execution, they are encoded to reduce memory footprint. In terms of dense CNN accelerator designs, streaming architectures are considered more efficient [7], as the layerwise hardware customisation and pipelining leads to a lower memory footprint and higher throughput. However, of all the prior streaming architecture works none have exploited postactivation sparsity. Streaming architectures pose the following challenges with regard to post-activation sparsity:

• Dynamic Scheduling: As the appearance of zeros is only known at run-time, a dynamic scheduler [8], [9] is required





Fig. 1: Comparison of our work against existing dense and sparse accelerators in terms of performance density (GOP/s/DSP). Details can be found in Table III.

to skip zeros and dispatch the remaining non-zero elements to computation units on-the-fly.

- Data Stream Synchronisation: Multiple data streams are processed in parallel for high throughput. However, the density and distribution of zeros across the feature maps vary, leading to an imbalanced workload between data streams which causes pipeline stalls. Load balancing and buffering are required.
- Resource Allocation: The allocation of FPGA resources to the various compute engines for a given performance target is a non-convex problem. Existing algorithms [10] provide solutions for the case of multiple dense computation engines, but sparse computation engines have not yet been considered.

In this work, a toolflow that generates streaming architecture is proposed which addresses the preceding research questions. The major contributions of our work include:

- A scalable, dynamically scheduled architecture design which can exploit post-activation sparsity.
- A compile-time workload balancing strategy and automated buffer sizing methodology to reduce pipeline stalls.
- A novel Design Space Exploration (DSE) method which considers measured sparsity distribution for balancing the rates of multiple sparse engines.

Over a set of CNN benchmarks, the results show that our approach can achieve $1.52 \times$ to $1.85 \times$ performance density compared to existing streaming dense architecture, and $1.41 \times$ to 1.93× performance density compared to state-of-the-art instruction-based sparse accelerators.

TABLE I: Comparison between our work and related works. Our work is the first to exploit post-activation sparsity on streaming architectures, with a novel DSE method that considers sparsity statistics. We also avoid the overhead of sparse encoding with dynamic scheduling.

Approach	[14]	[15]	[16]	[11]	[6]	[12]	[13]	Ours
Streaming	×	X	1	~	×	×	X	1
Sparsity	×	×	×	×	1	 Image: A second s	\checkmark	1
Encoding	×	×	×	×	\checkmark	1	×	×
DSE	1	1	×	1	×	×	×	1

II. RELATED WORKS

CNN Accelerators can generally be placed into two categories [7]: instruction-based architectures and streaming architectures. Instruction-based architectures [17], [18] use microinstructions to execute layers of the CNN model, typically with a systolic array hardware design for computation. These architectures are able to generalise across multiple CNN models, however, are limited by the inefficient processor-like control mechanisms. Streaming architectures are characterised by their deeply pipelined hardware, where every layer of the CNN is mapped to a dedicated computation engine. FPGAConvNet [11], FINN [19] and HLS4ML [20] are examples of toolflows which automate the generation of streaming architecture designs for a given target platform. This design method often achieves high-performance designs, as the workload is tailored to the available resources of the platform. However, these existing tools do not exploit post-activation sparsity as they are statically scheduled.

Sparse CNN accelerators have been explored in several works, especially on weight sparsity [21], [22], as the deterministic patterns of non-zero operations can be scheduled in a static manner. However, when dealing with post-activation sparsity, the presence of zeros is neither evenly distributed nor compile-time known, which poses a unique challenge for hardware designs. Existing research into exploiting postactivation sparsity has focused on two directions: skipping zero operations for energy savings, and using sparse representations for performance gains. For energy saving, zero-gating unnecessary computation to leave the arithmetic circuitry idle leads to greater energy efficiency [6], however, there are no performance benefits. Works that do exploit post-activation sparsity for performance gains require the data to be encoded in a sparse representation [23], [24]. By using representations such as Compressed Sparse Row (CSR) [23], non-zero operations can be routed to arithmetic circuits in a fine-grained manner. However, the overheads associated with sparse encoding are not scalable, making this approach only suited to extremely sparse workloads [25]. Furthermore, this approach has only been explored with instruction-based architectures, whose underlying hardware does not have the same performance benefits and challenges as streaming architectures. This work is the first to address the challenge of exploiting post-activation sparsity for performance gains in streaming architectures whilst utilising the original dense representation of the feature maps by designing a novel matrix-vector hardware which is dynamically scheduled.



Fig. 2: Diagram of the proposed Sparse Matrix-Vector Engine for $K_x, K_y = 2$ and k = 3. The *Non-Zero Check (NZC)* hardware generates a signal indicating if the feature map is non-zero.

III. ARCHITECTURE

In this section, the architecture of the proposed accelerator is described. The hardware design follows a streaming architecture approach.

A. Sparse Matrix-Vector Engine

The key operation being performed in streaming architecture accelerators is matrix-vector multiplication. In order to exploit sparsity in matrix-vector multiplication for performance gains, a novel Sparse Matrix-Vector Engine (S-MVE) is proposed. A diagram of the proposed hardware is given in Fig. 2. The hardware accepts streams of consecutive pairs of vectors from the sliding window module and weights memory. Each pair of feature map and weight elements is evaluated with a Non-Zero Check (NZC) module, which indicates the presence of non-zero inputs. The vector pairs are then fed into a Sparse Crossbar module along with the NZC flags. This module squeezes the $K_{\rm x} \times K_{\rm y}$ inputs to k outputs, and only routes the non-zero values to the crossbar output. The crossbar output feeds the non-zero values to k parallel MAC units, which perform the non-zero products. The products are then accumulated through an adder tree. Additional logic is required to handle extremely dense inputs, where the accumulation takes multiple cycles.



Fig. 3: Performance of the proposed Sparse Matrix-Vector Engine against sparsity for a typical $K_x, K_y = 3$ kernel size, across all MAC configurations. With the increasing sparsity, fewer MACs are required to achieve the maximum performance.

The performance characteristics of the proposed S-MVE are given in Fig. 3 for a typical $K_x, K_y = 3$ kernel size, across all the different MAC configurations. It can be seen that allocating more MACs to our engine leads to greater

performance, but with increasing sparsity, the performance gain per MAC diminishes. For a sparsity level greater than 40%, our implementation is always more resource-efficient than an equivalent dense implementation, achieving the maximum performance with fewer MACs allocated. Therefore, our hardware exposes a fine-grained trade-off between performance and MAC resources at different sparsity levels.



Fig. 4: LUT and FF resource usage as well as achieved clock frequency for a typical K_x , $K_y = 3$ kernel size, across all MAC configurations, synthesised for a Zynq-Ultrascale+ FPGA architecture. The design is able to maintain a frequency above 190MHz for all MAC configurations.

Furthermore, the utilisation characteristics and achieved clock frequency of the S-MVE hardware are explored in Fig. 4. For the proposed S-MVE, all the configurations are able to achieve a clock frequency above 190MHz, with up to 340MHz for extremely sparse hardware. The frequency dips towards the middle configuration, as this configuration contains the most complex crossbar with regard to routing. There is a steady increase in LUT and FF resources as the number of allocated MACs increases, however this relationship plateaus around the 5-MAC configuration. The LUT overheads mainly come from the sparse crossbar, and are not significant considering the savings on MACs. For reference, the cost of implementing a 16-bit MAC is 305 LUTs for the given FPGA fabric.

B. Pipelined Convolutional Layer

Fig. 5 illustrates the pipelined design inside a single convolutional layer as well as the integration of the S-MVE module. The hardware components are as follows:

- Sliding Window, which generates windows of the feature map from a single incoming stream by using line buffers.
- *Sparse Matrix-Vector Engine* takes as input the incoming feature map windows and corresponding weights, and performs the non-zero dot-products within the kernel dimensions of the convolution.
- Accumulator, which sums across the channel dimension.
 Bias Module, which adds a per-channel bias term.

Apart from the kernel parallelism within the S-MVE module denoted by k, the convolutional layer hardware also exploits input-channel and output-channel parallelism with the factors denoted as N_{I} and N_{\circ} respectively in the Fig. 5. Overall, there are $N_{I} \cdot N_{\circ}$ S-MVE modules computing in parallel within each convolutional layer. The communication between S-MVE modules is asynchronous as the instantaneous sparsity can be different across data streams, therefore synchronisation barriers are required, as illustrated in the figure.



Fig. 5: A block diagram of a convolutional layer within a streaming architecture design. The input channel parallelism $(N_{\rm I})$ and output channel parallelism $(N_{\rm O})$ are highlighted. The synchronisation boundaries required are also shown.

TABLE II: Taxonomy of symbols used in this paper.

Symbols	Definitions
B	batch size of feature map
L	total layers in the network
C_{I}, C_{O}	number of channels into and out of the layer
H_{\circ}, W_{\circ}	spatial dimensions of the output feature map
$K_{ m x}, K_{ m y}$	height and width of convolution kernel
$N_{ m I}, N_{ m O}$	input and output channel parallelism
k	number of MACs inside each S-MVE, $k \leq K_{\rm x}K_{\rm y}$

IV. DESIGN SPACE EXPLORATION

Elaborating on sparsity, it is the measure of the number of zero values in a stream of observed data. In this paper, we use s_m to denote the instantaneous sparsity within the m_{th} stream. The average sparsity is the expected value of the sparsity distribution ($\bar{s}_m = \mathbb{E}[s_m]$). All these statistics are measured on a subset of ImageNet validation data.

In this section, the DSE problem of finding a maximal throughput hardware design for a given CNN model and FPGA pair is discussed. Our DSE method decides the allocation of MACs based on the average sparsity (section IV-A), as well as the insertion of buffers based on the variation of sparsity (section IV-B). Table II gives the taxonomy of symbols used.

A. MAC Allocation

In our design, all the MAC units are implemented with the DSP resources on the FPGA. As each convolutional layer is mapped to $N_{\rm I} \cdot N_{\rm O}$ S-MVE, each containing k MAC units, the per-layer DSP utilisation is modelled using the following equation.

$$\mathcal{R}_{DSP} = N_{\mathrm{I}} \cdot N_{\mathrm{O}} \cdot k \tag{1}$$

In streaming architectures, the average throughput of the whole system is dictated by the slowest layer. Therefore, the allocation of DSP resources is guided by the performance modelling of S-MVE. As each S-MVE is responsible for computing the kernel dimensions of the convolution, the average number of non-zero MAC operations required to produce one output is $(1 - \bar{s}_m) \cdot K_x \cdot K_y$.

As each S-VPE contains k MACs, its average throughput can be expressed as,

$$\bar{\theta}_{m,n} = \min\left(1, \frac{k}{(1-\bar{s}_m) \cdot K_{\mathrm{x}} \cdot K_{\mathrm{y}}}\right) \tag{2}$$

The performance increases as sparsity increases up to the maximum throughput of 1 element per cycle for each S-VPE. This model drives the sparsity-resource trade-off, where achieving maximum throughput does not necessarily require $K_x \cdot K_y$ MACs, and the saved resources can be allocated to other slower stages of the pipeline. The S-MVE performance models can be used to construct the average latency, \bar{t}_i , of a convolutional layer,

$$\bar{t}_i = H_{\circ} \cdot W_{\circ} \cdot \frac{C_{\scriptscriptstyle \rm I}}{N_{\scriptscriptstyle \rm I}} \cdot \frac{C_{\circ}}{N_{\circ}} \cdot \left(\max_{m \in [1,N_{\scriptscriptstyle \rm I}], n \in [1,N_{\circ}]} \frac{1}{\bar{\theta}_{m,n}} \right)$$
(3)

Given adequate buffering (as discussed in Section IV-B), the latency of the layer is dictated by the slowest S-MVE. Finally, the MACs allocation is expressed as the following optimisation problem:

$$\max\min_{i\in[1,L]}\frac{B}{\overline{t_i}}, \ s.t.\sum_i \mathcal{R}_{DSP} \le budget$$
(4)

where L is the number of layers and B is the batch size. This optimisation problem is solved using the simulated annealing algorithm [10].

B. Buffer Depth Sizing

The above performance modelling in (2) and (3) assumes zero variance in each stream, which underestimates the latency given *Jensen's inequality* that states $t(\mathbb{E}[\theta]) \leq \mathbb{E}[t(\theta)]$. From the hardware perspective, latency underestimation is caused by back-pressure from the synchronisation barriers illustrated in Fig. 5, where the observed instantaneous sparsity deviates from its average value. It is therefore necessary to introduce buffering that reduces the *Jensen gap* between estimated and actual latency.

Buffers are placed at the input of S-MVEs, accounting for variations in instantaneous sparsity between the S-MVE input streams. In order to determine a suitable choice in buffer depth, a statistical method based on the calculation of a moving average of sparsity is proposed, which is given as,

$$\psi_m^w(j) = \frac{1}{w} \sum_{i=j}^{j+w} s_m(i)$$
(5)

 ψ_m^w is the time series for the moving average of stream m for a window size of w, and s_m is the time series of the sparsity observed on stream m. The intuition is that as the buffer size increases, the detrended average value of samples in the buffers converge to the average sparsity level of the stream.

To measure the impact of buffer sizing, the *back pressure metric*, ρ_w is proposed, which is defined as,

$$\rho_w = \mathbb{E}\left[\max_m \psi_m^w - \min_m \psi_m^w\right] - \left(\max_m \bar{s}_m - \min_m \bar{s}_m\right) \quad (6)$$

This metric gives the average maximum difference between the moving average windows, reflecting the average number



Fig. 6: Comparison of the back-pressure metric and observed latency overhead for different buffer sizes, for the 2^{nd} layer of ResNet-18 with a configuration of $N_I = 32$ and k = 1. The cost of the buffer in terms of LUTRAM is given for each buffer size.

of extra samples needed to balance the workload in that period. The difference in average sparsity between the most and least sparse streams is subtracted to normalise for unbalanced streams. The greater ρ_w is, the slower the execution of the hardware will be with respect to (3).

The effectiveness of the back pressure metric at identifying the optimal buffer size is evaluated in Fig. 6. It can be seen that the metric is strongly correlated with the latency overhead observed. The buffer size is chosen based on a stopping condition for ρ_w as well as a limit on LUTRAM.

V. EVALUATION

In this section, the performance and resource utilisation of the proposed framework is evaluated. For hardware synthesis, Vivado 2020.1 is used.

A. Dense vs Sparse Design Comparison

The performance benefits of sparsity on the proposed architecture are evaluated in this subsection. The proposed toolflow is used to generate both dense designs using an existing Matrix-Vector Engine [11], as well as designs with the proposed Sparse Matrix-Vector Engine.

Fig. 7 illustrates the dense and sparse hardware performance for a set of representative CNN workloads: AlexNet [26], VGG11 & VGG16 [27], RepVGG-AO [3], MobilenetV2 [28] and ResNet-18 & ResNet-50 [29]. The sparse engine exceeds the performance of the dense engine for all CNN models. The largest gain was observed for ResNet-18 (51%), whereas the smallest was for MobileNetv2 (9%). For both MobileNetV2 and ResNet-50, the performance gains realised were marginal. In the case of MobileNetV2, this is due to most of the workload being point-wise convolutions, as the proposed S-MVE hardware is not able to exploit the sparsity of 1×1 kernels. For ResNet-50, both dense and sparse designs are constrained by the large on-chip memory requirements, bottlenecking their achievable performance. Overall, the proposed toolflow is able to exploit the post-activation sparsity leading to significant performance gains.

The performance improvements for the sparse architecture can be attributed to sparsity. For example, the average sparsity across all the convolutional layers of VGG16 and ResNet-18 is

TABLE III: Comparison of the performance and resources of related works for CNN models running ImageNet. We use GOP/s/DSP to evaluate the performance with a normalised hardware resource since other approaches use different FPGA devices. The best result in each comparison is highlighted in bold and green. W. = weights, and P.-A. = post activation.

	[11]	[12]	[13]	[6]	Ours	Ours	[11]	[14]	Ours	[13]	Ours
Network			VG	G16				ResNet-18		ResNo	et-50
Quantisation	W16A16	W8A16	W16A16	W16A16	W16A16	W16A16	W16A16	W16A16	W16A16	W16A16	W16A16
Sparsity	-	-	W.	W., PA.*	PA.	PA.	-	-	PA.	W.	PA.
Streaming	Yes	No	No	No	Yes	Yes	Yes	No	Yes	No	Yes
Device	ZC706	VC709	ZCU102	ZCU102	ZC706	ZCU102	ZC706	ZC706	ZC706	ZCU102	ZCU102
Freq. (MHz)	200	200	200	200	200	200	200	150	200	200	200
LUT (k)	148 (68%)	121 (28%)	252 (92%)	178 (65%)	120 (55%)	163 (59%)	147 (67%)	164 (75%)	129 (59%)	252 (92%)	260 (95%)
BRAM	798 (73%)	934 (32%)	912 (50%)	1460 (80%)	504 (46%)	912 (50%)	528 (48%)	948 (87%)	586 (54%)	912 (50%)	1382 (76%)
DSP	603 (67%)	664 (18%)	1144 (45%)	1350 (53%)	512 (57%)	1024 (41%)	588 (65%)	900 (100%)	528 (59%)	1144 (45%)	1032 (41%)
GOP/s	198.0	230.1	309	495.4	310.8	534.4	135.0	181.6	185.4	291.4	252.7
GOP/s/DSP	0.33	0.35	0.27	0.37	0.61	0.52	0.23	0.20	0.35	0.25	0.24



Fig. 7: Performance comparison between the dense streaming accelerator and the proposed sparse streaming accelerators for representative CNN workloads, targeting a U250 FPGA. Our tool generates designs with up to 50% greater performance.

0.65 and 0.57 respectively for the ImageNet validation dataset. This suggests 1/(1-0.65) = 2.86 and 1/(1-0.57) = 2.32 speed-up at maximum. The gap between the theoretical maximum speed-up and the improvement achieved is due to the overhead on clock frequency and LUT usage, as described in Section III-A.

A detailed comparison between the dense and sparse engines focusing on the 3rd convolutional layer of VGG16 is given in Table IV, which is representative for many 3×3 convolutional layers across CNN models. The results demonstrate the performance benefits of the proposed S-MVE module, as it is able to effectively bypass zero multiplications, reducing the latency by 60%. At the same time, the clock frequency and LUT usage are penalised by 10% and 50% receptively, creating different bottlenecks during the DSE for the entire network.

TABLE IV: A case study comparing dense and sparse architectures for the 3^{rd} convolutional layer of VGG16. The sparse hardware achieves better performance with the overhead on LUT, FF and frequency.

Design	LUT	FF	BRAM	DSP	Freq. (MHz)	Lat. (ms)
Dense	26,046	41,211	272	192	223	44.5
Sparse	38,112	48,895	272	192	200	17.8
	1.5 ×	1.2 ×	1.0 imes	1.0 imes	0.9 ×	0.4 ×

B. Comparing with Existing Sparse Accelerators

In Table III, our work is evaluated against both instructionbased sparse accelerators [13], [6], as well as a state-of-theart streaming but dense accelerator [11]. For sparse works, we achieved up to $1.93 \times$ GOP/s/DSP on VGG16, which demonstrates the benefit of combining post-activation sparsity exploitation and streaming. Compared to a high-performance streaming architecture [11], our work achieves $1.85 \times$ and $1.52 \times$ GOP/s/DSP on VGG16 and ResNet-18 respectively, without any degradation on the network accuracy. This reiterates the impact sparsity has on performance.

Our hardware is not able to outperform [13] on ResNet-50 due to the limited LUT resources. We observe that both our design and the design in [13] are LUT-bounded, however, compared with their instruction-based architecture, streaming architectures require extra buffers for weight storage and pipelining between layers, consuming additional LUTRAM and BRAM. From table III, our design uses 4% less DSP than [13], yet consumes 3% more LUT and 26% more BRAM comparatively. Therefore, in order to fully exploit the potential of our design, devices with more on-chip memory resources are desirable.

VI. CONCLUSION

In this work, a toolflow is proposed for exploiting postactivation sparsity in streaming-based CNN accelerators. We address the key challenges which arise from non-deterministic sparse execution including dynamic scheduling, data stream synchronisation and statistics-aware design space exploration. Overall, our method can achieve $1.41 \times$ to $1.93 \times$ greater performance compared to existing instruction-based sparse accelerators. With regard to future work, we are exploring the opportunity of CNN-accelerator co-design, such as encouraging input-sparsity of the slowest layer in the pipeline through a sparsity regulariser.

ACKNOWLEDGEMENTS

For the purpose of open access, the authors have applied a Creative Commons Attribution (CC BY) license to any Accepted Manuscript version arising.

REFERENCES

- A. Kolesnikov, A. Dosovitskiy, D. Weissenborn, G. Heigold, J. Uszkoreit, L. Beyer, M. Minderer, M. Dehghani, N. Houlsby, S. Gelly, T. Unterthiner, and X. Zhai, "An image is worth 16x16 words: Transformers for image recognition at scale," 2021.
- [2] A. Howard, M. Sandler, G. Chu, L.-C. Chen, B. Chen, M. Tan, W. Wang, Y. Zhu, R. Pang, V. Vasudevan *et al.*, "Searching for mobilenetv3," in *Proceedings of the IEEE/CVF international conference on computer* vision, 2019, pp. 1314–1324.
- [3] X. Ding, X. Zhang, N. Ma, J. Han, G. Ding, and J. Sun, "Repvgg: Making vgg-style convnets great again," in *Proceedings of the IEEE/CVF* conference on computer vision and pattern recognition, 2021, pp. 13733– 13742.
- [4] J. Li, S. Jiang, S. Gong, J. Wu, J. Yan, G. Yan, and X. Li, "Squeezeflow: A sparse cnn accelerator exploiting concise convolution rules," *IEEE Transactions on Computers*, vol. 68, no. 11, 2019.
- [5] A. Gondimalla, N. Chesnut, M. Thottethodi, and T. Vijaykumar, "Sparten: A sparse tensor accelerator for convolutional neural networks," in *Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture*, 2019, pp. 151–165.
- [6] C. Zhu, K. Huang, S. Yang, Z. Zhu, H. Zhang, and H. Shen, "An efficient hardware accelerator for structured sparse convolutional neural networks on fpgas," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 9, 2020.
- [7] S. I. Venieris, A. Kouris, and C.-S. Bouganis, "Toolflows for mapping convolutional neural networks on FPGAs: A survey and future directions," *ACM Computing Surveys*, vol. 51, no. 3, 2018.
- [8] J. Cheng, L. Josipovic, G. A. Constantinides, P. Ienne, and J. Wickerson, "Combining dynamic & static scheduling in high-level synthesis," in *Proceedings of the 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, 2020.
- [9] L. Josipović, A. Marmet, A. Guerrieri, and P. Ienne, "Resource sharing in dataflow circuits," in 2022 IEEE 30th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2022.
- [10] A. Montgomerie-Corcoran, Z. Yu, and C.-S. Bouganis, "Samo: Optimised mapping of convolutional neural networks to streaming architectures," in 2022 32nd International Conference on Field-Programmable Logic and Applications (FPL). IEEE, 2022, pp. 418–424.
- [11] S. I. Venieris and C.-S. Bouganis, "fpgaconvnet: Mapping regular and irregular convolutional neural networks on fpgas," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 30, no. 2, 2019.
- [12] J. Li, K.-F. Un, W.-H. Yu, P.-I. Mak, and R. P. Martins, "An fpga-based energy-efficient reconfigurable convolutional neural network accelerator for object recognition applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 9, 2021.
- [13] L. Lu, J. Xie, R. Huang, J. Zhang, W. Lin, and Y. Liang, "An efficient hardware accelerator for sparse convolutional neural networks on fpgas," in 2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2019.
- [14] S. I. Venieris, J. Fernandez-Marques, and N. D. Lane, "unzipfpga: Enhancing fpga-based cnn engines with on-the-fly weights generation," in 2021 IEEE 29th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM). IEEE, 2021, pp. 165–175.
- [15] H. Sharma, J. Park, E. Amaro, B. Thwaites, P. Kotha, A. Gupta, J. K. Kim, A. Mishra, and H. Esmaeilzadeh, "Dnnweaver: From high-level

deep network models to fpga acceleration," in the Workshop on Cognitive Architectures, 2016.

- [16] A. Sohrabizadeh, J. Wang, and J. Cong, "End-to-end optimization of deep learning applications," in *Proceedings of the 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, 2020.
- [17] N. P. Jouppi, C. Young, N. Patil, D. Patterson, G. Agrawal, R. Bajwa, S. Bates, S. Bhatia, N. Boden, A. Borchers *et al.*, "In-datacenter performance analysis of a tensor processing unit," in *Proceedings of the 44th annual international symposium on computer architecture*, 2017, pp. 1– 12.
- [18] L. Liu and S. Brown, "Leveraging fine-grained structured sparsity for cnn inference on systolic array architectures," in 2021 31st International Conference on Field-Programmable Logic and Applications (FPL). IEEE, 2021, pp. 301–305.
- [19] M. Blott, T. B. Preußer, N. J. Fraser, G. Gambardella, K. O'brien, Y. Umuroglu, M. Leeser, and K. Vissers, "Finn-r: An end-to-end deeplearning framework for fast exploration of quantized neural networks," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 11, no. 3, 2018.
- [20] J. Duarte, S. Han, P. Harris, S. Jindariani, E. Kreinar, B. Kreis, J. Ngadiuba, M. Pierini, R. Rivera, N. Tran, and Z. Wu, "Fast inference of deep neural networks in FPGAs for particle physics," *Journal of Instrumentation*, vol. 13, no. 07, 2018.
- [21] W. You and C. Wu, "Rsnn: A software/hardware co-optimized framework for sparse convolutional neural networks on fpgas," *IEEE Access*, vol. 9, 2021.
- [22] L. Lu and Y. Liang, "SpWA: An efficient sparse winograd convolutional neural networks accelerator on FPGAs," in 2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC), 2018.
- [23] A. Parashar, M. Rhu, A. Mukkara, A. Puglielli, R. Venkatesan, B. Khailany, J. Emer, S. W. Keckler, and W. J. Dally, "Scnn: An accelerator for compressed-sparse convolutional neural networks," in *Proceedings of the 44th Annual International Symposium on Computer Architecture*, 2017.
- [24] A. Gondimalla, N. Chesnut, M. Thottethodi, and T. N. Vijaykumar, "Sparten: A sparse tensor accelerator for convolutional neural networks," in *Proceedings of the 52nd Annual IEEE/ACM International Symposium* on Microarchitecture, 2019.
- [25] Y. Liang, L. Lu, and J. Xie, "Omni: A framework for integrating hardware and software optimizations for sparse cnns," *IEEE Transactions* on Computer-Aided Design of Integrated Circuits and Systems, vol. 40, no. 8, pp. 1648–1661, 2020.
- [26] A. Krizhevsky, I. Sutskever, and G. E. Hinton, "Imagenet classification with deep convolutional neural networks," *Commun. ACM*, 2017.
- [27] K. Simonyan and A. Zisserman, "Very deep convolutional networks for large-scale image recognition," in 3rd International Conference on Learning Representations, ICLR 2015, San Diego, CA, USA, May 7-9, 2015, Conference Track Proceedings, 2015.
- [28] A. G. Howard, M. Zhu, B. Chen, D. Kalenichenko, W. Wang, T. Weyand, M. Andreetto, and H. Adam, "Mobilenets: Efficient convolutional neural networks for mobile vision applications," *arXiv preprint* arXiv:1704.04861, 2017.
- [29] K. He, X. Zhang, S. Ren, and J. Sun, "Deep residual learning for image recognition," 2015.